REMARKS

Applicants respectfully request the Examiner's reconsideration of the present application.

Claims 1, 3, and 5-22 in the present application are pending.

Claims 1, 3, and 5-22 are rejected under 35 U.S.C. § 112, first paragraph.

Claims 1, 3, and 5-22 are rejected under 35 U.S.C. § 101.

Claims 1, 3, 5-7, 9, and 11-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,711,602 ("Bhandal") in view of U.S. Patent No. 7,046,723 ("Schier").

No art rejections were provided for claims 8 and 10.

Claims 1, 11, 17, 21, and 22 have been amended. Support for the amendment to claims may be found in paragraphs [0005] and [0028]-[0047], Figures 2-5, and claims 1-20 as originally filed. No new matter has been added.

Claims 1, 3, and 5-22 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

As stated above, claims 1, 11, 17, 21, and 22 have been amended. The language "performing multiplication of a first number with a second number on a field programmable gate array utilizing a digital signal processor (DSP) configured to multiply only a subset of a number of bits forming the first and second numbers" is supported by the specification.

For example, the specification provides the following description.

> [0005] Memory blocks on a FPGA are used to extend the resolution of a DSP block multiplier. For an n*m bit multiplier configuration, the DSP block is used to implement only a subset of the n*m bit multiplication functions. The remaining multiplication functions may be implemented by one or more memory blocks. A memory block may be used to store values that result from n*m bit multiplication functions not performed by the DSP block.

(Paragraph [0005] of the Specification) (Emphasis Added).

> [0026] Components on the FPGA 100 may be used to implement an n*m bit multiplier. The multiplier may include a DSP block and one or more memory blocks in the FPGA 100. In one embodiment, the DSP block is used to generate a product (a first decomposition product) by multiplying a first plurality of the n bits from a first number and a first plurality of m bits from a second number. The memory block is used to store values that represent all the combinations of multiplying a second plurality of the n bits from the first number and a second plurality of the m bits from the second number.

(Paragraph [0026] of the Specification) (Emphasis Added).

> [0028] ... In one embodiment, the largest dimension supported by the DSP block that is under the desired multiplier configuration is selected. It should be appreciated that if the largest dimension supported by that is under the desired multiplier configuration is not available, a smaller dimension supported by the DSP block may also be selected. The DSP block may be configured to generate a product by performing multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number.

(Paragraph [0028] of the Specification) (Emphasis Added).

> [0033] At 205, offsets are determined for the decomposition products from the resources. Because decomposition products represent the products of subsets of bits from the first number and subsets of bits from the second number, the decomposition products need to be scaled to reflect their true values. Offsets may be used to scale the decomposition products. According to an embodiment of the present invention, an offset for a decomposition value may be determined from the position of its corresponding subset of bits from the first number and the position of its corresponding subset of bits from the second number.

(Paragraph [0033] of the Specification) (Emphasis Added).

> Figure 5 illustrates an exemplary multiplier bit map 500 for a 10*12 multiplier configuration according to a first embodiment of the present invention. As mapped on the multiplier bit map 500, a DSP block 510 that is configured to support 9*9 bit multiplication is designated to multiply the 9 most significant bits of a first number with the most 9 most significant bits of the second number.

(Paragraph [0040] of the Specification) (Emphasis Added).

> Figure 6 illustrates an exemplary multiplier bit map 600 for a 10*12 multiplier configuration according to a second embodiment of the present invention. As mapped on the multiplier bit map 600, a DSP block 610 that is configured to support 9*9 bit multiplication is designated to multiply the 9 least significant bits of a first number with the 9 least significant bits of the second number.

(Paragraph [0041] of the Specification) (Emphasis Added).

Applicants submit that amended claims 1, 11, 17, 21, and 22 comply with the enablement requirement of 35 U.S.C. §112, first paragraph as well as 35 U.S.C. §132(a). No new matter has been added.

Claims 1-3, and 5-22 are rejected under 35 U.S.C. § 101.

In the Office Action mailed 11/13/2008, the Office states in part that

> Claims 1, 3 and 5-22 cite a method and device for performing multiplication in accordance with a predetermined mathematical algorithm. However, claims 1, 3 and 5-22 merely disclose series of steps for performing sum of shift products without providing a practical application. In addition, claims 1, 3, and 5-22 appear to preempt every substantial practical application of the idea embodied by the claims. The method claims 1, 3, 5-16 and 21 must also tight (sic) or direct to another statutory class as hardware for realizing the implementation. Therefore, claims 1, 3 and 5-22 are directed to non-statutory subject matter.

(11/13/2008 Advisory Action, p. 3).

Applicants respectfully disagree. The United States Court of Appeals, Federal Circuit has articulated recently that "A patent claim that is tied to a particular machine or brings about a particular transformation of a particular article does not pre-empt all uses of a fundamental principle in any field but rather is limited to a particular use, a specific application; therefore, it is not drawn to the principle in the abstract" In re Bilski, 545 F.3d 943, 954 (Fed.Cir.2008).

Applicants submit that claims 1, 3, and 5-22 do not "merely disclose [a] series of steps for performing sum shift products" as the Office suggests. Instead, claims 1, 11, and 21 are tied to a field programmable gate array, a digital signal processor, and a memory. Furthermore, claims 17 and 22 are apparatus claims directed to multipliers that are tied to a digital signal

processor and a memory. Each claim that is pending includes hardware limitations. Applicants submit that claims 1, 3, and 5-22 clearly satisfy the requirements of being statutory subject matter under 35 U.S.C. §101.

Claims 1, 3, 5-7, 9, and 11-22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over 6,711,602 ("Bhandal") in view of U.S. Patent 7,046,723 ("Schier").

It is submitted that Bhandal and Schier do not render claims 1, 3, 5-7, 9, and 11-22 unpatentable under 35 U.S.C. §103(a).

Bhandal includes a disclosure of a pair of parallel 16.times.16 multipliers each with two 32-bit inputs and one 32-bit output. There are options to allow input halfword and byte selection for four independent 8x8 or two independent 16x16 multiplications, real and imaginary parts of complex multiplication, pairs of partial sums for 32x32 multiplication, and partial sums for 16x32 multiplication. There are options to allow internal hardwired routing of each multiplier unit results to achieve partial-sum shifting as required to support above options. There is a redundant digit arithmetic adder before final outputs to support additions for partial sum accumulation, complex multiplication vector accumulation and general accumulation for FIRs/IIRs--giving MAC unit functionality. There are options controlled using bit fields in a control register passed to the multiplier unit as an operand. There are also options to generate all of the products needed for complex multiplication (see Bhandal Abstract).

Schier includes a disclosure of a digital and a multiplication method are described, which lead to an efficient architecture for a hardware implementation of digital FIR and IIR filters into FPGAs. The multiplications of input sample data and delayed sample data with filter coefficients are performed by addressing look-up tables in which corresponding multiplication results are prestored. The size of the look-up tables is reduced by storing only those multiplication results which cannot be obtained by a shifting operation performed on the other pre-stored multiplication results, the input sample data, or the delayed sample data. Thereby, the

size of the look-up tables can be compressed significantly such that an implementation of large digital filters into FPGAs is possible (see Schier Abstract).

It is submitted that Bhandal and Schier do not teach or suggest a method for performing multiplication of a first number with a second number on a field programmable gate array utilizing a single digital signal processor (DSP) configured to multiply only a subset of a number of bits forming the first and second numbers that includes generating a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number using the DSP configured to perform multiplication on a fewer number of bits then those forming the first and second numbers, retrieving a stored value designated as a product of a second plurality of bits from the first number and a second plurality of bits from the second number from a memory, scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number, and summing a scaled product and a scaled stored value to generate a value representing a product of the first number and the second number, wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits.

In the Office Action mailed 11/13/2008, the Office has stated in part that

> The applicant argues in pages 9-11 for claims that primary reference by Bhandal fails to disclose a multiplier that is configured to perform multiplication on all the number of bits used for forming the first [and] second numbers being multiplied, and is not using a multiplier that is configured to perform multiplication on a fewer number of bits than those forming the first and second numbers. In addition, the Schier teaches away from combining a DSP multiplier such as described in Bhandal.
>
> The examiner respectfully submits that the above alleged limitations is clearly seen directly in Figures 11B or 11D by Bhandal wherein the multiplication is performed to multiply source 1 with source 2 but producing only half of the size of the actual bits of the multiplication. Thus, Figure 11B or 11D clearly meets the claim language. For the combination, neither

> Bhandal nor Schier discloses explicitly that it cannot be combined with other reference to form the claim invention.

(11/13/2008 Office Action, p. 15)

Applicants respectfully disagree. Bhandal discloses a processor utilizing a pair of 16x16 multipliers each with two 32-bit inputs and one 32-bit output to perform 32x32 multiplication. Bhandal discloses options to allow internal hardware routing of each multiplier unit results to achieve partial-sum shifting to support 32x32 multiplication (see Bhandal column 2, lines 53-65 and column 22, lines 17-26). As illustrated in Figures 11A-11D, the higher bits from source 1 (A) is multiplied with the higher bits from source 2 (C) while the lower bits of source 1 (B) is multiplied with the lower bits of source 2 (D). All of the bits from sources 1 and 2 are multiplied (see Bhandal Figures 11A-11D). Thus, by utilizing a pair of multipliers, Bhandal discloses a processor configured to multiply more than a subset of number of bits forming a first and second numbers. Bhandal generates a product by using a pair of multipliers in a processor to perform multiplication on all of the bits forming the first and second numbers.

In the response filed September 1, 2008, Applicants presented reasons why the combination of Bhandal and Schier would be improper. Applicants disagreed with the Office's motivation for the combining because "it would have been obvious to a person having ordinary skill in the art at the time of the invention is made to add ... the second product ... retrieved from a memory as seen in Schier... because it would ... improve system performance." In the example disclosed in Bhandal, the number of bits of the numbers being multiplied, 32, match the configuration of the number of bits multiplied by multipliers 800 and 801, 32. Thus, there is no need or motivation to add a further product from memory. Furthermore, because there is a match, there would be no improvement in system performance. In fact, by requiring a stored product to be added, the multiplier in Bhandal would have its performance worsen not improve.

Applicants also submitted that "the intermediate product from the LUT in Figures 1-4" of Schier could not be arbitrarily used as "the second product" as the Office suggests on page 4

of the Office Action mailed 4/1/2008. The Office states that both the product generated by the DSP and the stored value from memory are required to be scaled in Bhandal by the shifters 810 and 811 illustrated in Figure 8, whereas one of the objects of the Schier invention is to avoid shifting in maintain low latency.

In the Office Action mailed 11/13/2008, the Office states in part that

> The applicant argues in pages 12-13 that the invention by Schier does not require or permit the shifting which the Office is requiring for the "stored value" by shifter 811 in Figure 8 of Bhandal since the shifting would render the result incorrectly.
> The examiner respectfully submits that the previous Office action already stated clearly that the secondary reference does not need to show every limitation cited in the primary reference. Thus, the examiner only borrows or applied the feature or limitation from the secondary reference by Schier of having the second product from a memory as clearly addressed in the rejection above.

(11/13/2008 Office Action, p. 16).

Applicants respectfully submit that the Office has misunderstood Applicants position. Applicants are not stating that a secondary reference needs to show every limitation cited in a primary reference. Applicants are stating that when combining two references, if the proposed modification would render the prior art unsatisfactory for its intended purpose then there is no suggestion or motivation to make the proposed modification. This is also the holding of the Federal Circuit in its decision in In re Gordon, 733 F.2d 900 (Fed.Cir. 1984) (also see MPEP 2143.01 V). Schier clearly states in its Summary of the Invention, that one of the objects of the present invention is achieved by having its input sample data not divided into its bit position so that an additional shifting operation is not required after multiplication and a low latency is introduced (see Schier column 3, columns 3-11 and column 4, lines 3-12).

In contrast, claim 1 states

> A method for performing multiplication of a first number with a second number on a field programmable gate array utilizing a single digital signal processor (DSP) configured to multiply only a subset of a number of bits forming the first and second numbers, comprising:

> generating a product by multiplying a first plurality of bits from the first number and a first plurality of bits from the second number using the DSP configured to perform multiplication on a fewer number of bits then those forming the first and second numbers;
>
> retrieving a stored value designated as a product of a second plurality of bits from the first number and a second plurality of bits from the second number from a memory;
>
> scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number; and
>
> summing a scaled product and a scaled stored value to generate a value representing a product of the first number and the second number, wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits.

(Claim 1, as Amended) (Emphasis Added).

Claims 11, 17, 21, and 22 include similar limitations.

Given that claims 3, and 5-10 depend from claim 1, claims 12-16 depend from claim 11, and claims 18-20 depend from claim 17, it is likewise submitted that claims 3, 5-10, 12-16, and 18-20 are also patentable under 35 U.S.C. §103(a) over Bhandal and Schier.

In view of the arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1, 3, and 5-22 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicants' attorney (217-377-2500) to facilitate prosecution of this application.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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